REMARKS

The Official Action mailed August 8, 2006, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on January 16, 2002; and February 5, 2004.

Claims 1-7 are pending in the present application, of which claims 1, 2 and 7 are independent. Claims 1, 2 and 7 have been amended to better recite the features of the present invention. Claim 5 has been amended to correct minor informalities. The Applicant notes with appreciation the allowance of claims 3-6 (page 3, Paper No. 20060729). For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Paragraph 2 of the Official Action rejects claims 1, 2 and 7 as anticipated by U.S. Patent No. 6,683,921 to Shiraishi. The Applicant respectfully submits that an anticipation rejection cannot be maintained against the independent claims of the present application, as amended.

As stated in MPEP § 2131, to establish an anticipation rejection, each and every element as set forth in the claim must be described either expressly or inherently in a single prior art reference. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Independent claims 1 and 7 have been amended to recite absolute-phasing a PSK modulation signal in which the phase of a signal point is adjusted by a carrier regenerated by a carrier regenerating loop, where a phase of a signal point indicated by the PSK modulation signal absolute-phased by the absolute-phasing means (or in the step of absolute-phasing a PSK modulation signal) is shifted by a phase determined on the basis of the type of PSK modulation technique applied to a received signal and a phase error contained in the PSK modulation signal, then the digital signal is decoded,

and the carrier is regenerated on the basis of a phase error detected by performing burst receiving only in a predetermined signal interval. Independent claim 2 has been amended to recite phase shift means for shifting the phase of a signal point indicated by a PSK modulation signal absolute-phased by said absolute-phasing means by a phase determined on the basis of the type of PSK modulation technique applied to a received signal and a phase error contained in the PSK modulation signal. For the reasons provided below, the Applicant respectfully submits that Shiraishi '921 does not teach the above-referenced features of the present invention, either explicitly or inherently.

The BS digital broadcast receiver in accordance with the present invention accomplishes a stable receiving operation by shifting the phase of a signal point indicated by the I signal ADI1 and the Q signal ADQ1, which are absolute-phased after the phase error or the frequency error have been compensated by the carrier regenerating loop, by the phase corresponding to the modulation technique applied to the received signal and the phase error amount. Such processing enables a reduction in the effect on the error rate due to the phase noise of the outdoor unit (ODU), and enables the stable receiving operation by performing the burst receiving at all times regardless of the magnitude of the carrier-to-noise ratio (CNR) and by regenerating the carrier.

The BS digital broadcast receiver in accordance with the present invention comprises a complex calculator circuit 11, an FIR filter 12, a latch 13, an absolute-phasing section 14 a carrier regeneration phase error table 15, a loop filter 16, a numerical control frequency oscillator (NCO) 17, first to third filters 18 to 20, a selective complex calculator circuit 21, a frame synchronization pattern detector circuit 22, a decoding section 23, a TMCC decoding section 24, and a timing generator circuit 25.

In the BS digital broadcast receiver, a complex calculator circuit 11, an FIR filter 12, a latch 13, a carrier regeneration phase error table 15, a loop filter 16, and an NCO 17 constitutes a carrier regenerating loop for compensating for the frequency error of

the carrier included in the I signal component I0 and the Q signal component Q0 of the base band received from the quadrature detector or the like.

The complex calculator circuit 11 uses the sine wave data sin θ and the cosine wave data cos θ received from the NCO 17 so as to perform the following calculation, and generates the I signal component RI and the Q signal component RQ in which the phases are adjusted as follows:

$RI = I0 \times \cos\theta - Q0 \times \sin\theta$

$RQ = I0 \times \sin\theta + Q0 \times \cos\theta$.

The complex calculator circuit 11 feeds the generated I signal component RI and Q signal component RQ to the FIR filter 12, and the FIR filter 12 limits the band so as to generate the I signal component DI and Q signal component DQ. The carrier regeneration phase error table 15 identifies the signal point position in the signal space on the basis of the I signal component DI and the Q signal component DQ received from the latch 13, and generates a phase error signal PED representative of the phase error of the phase indicated by the signal point position and the absolute phase. The carrier regeneration phase error table 15 transmits the generated phase error signal PED to the loop filter I6. The loop filter 16 generates a phase adjustment signal $L\Delta f$ made by smoothing the phase error signal PED while switching the filtering/holding operation according to the timing signal BRTEN received from the timing generator circuit 25, and feeds it to the NCO 17. The NCO 17 generates the sine wave data sin θ and the cosine wave data cos θ to be accumulated (oscillated) corresponding to the phase adjustment signal $L\Delta f$, and transmits them to the complex calculator circuit 11. Thus, the carrier regenerating loop regenerates the carrier, and the phase synchronization is established.

The frame synchronization pattern detector circuit 22 transmits, to the absolute-phasing section 14, a signal indicating whether the value of each digit of the detected frame synchronization pattern W1 is reversed or not, that is, whether the detected frame synchronization pattern W1 is received at the absolute phase or at the phase shifted by

180 degrees from the absolute phase. When the absolute-phasing section 14 determines that the detected frame synchronization pattern W1 is received at the absolute phase on the basis of the signal received from the frame synchronization pattern detector circuit 22, the absolute-phasing section 14 remains the received I signal component DI and the received Q signal component DQ as they are as the I signal component ADI1 and the Q signal component ADQ2 so as to transmit the I signal component ADI1 and the Q signal component ADQ2 to the selective complex calculator circuit 21. That is, the absolute-phasing section 14 performs the following operation:

$ADI1 = DI \times \cos(0) - DQ \times \sin(0)$

$ADQ2 = DI \times \sin(0) + DQ \times \cos(0)$.

On the other hand, when the absolute-phasing section 14 determines that the detected frame synchronization pattern W1 is received at the phase shifted by 180 degrees from the absolute phase on the basis of the signal received from the frame synchronization pattern detector circuit 22, the absolute-phasing section 14 performs the absolute in accordance with the following operation:

$ADI1 = DI \times \cos(-\pi) - DQ \times \sin(-\pi)$

$ADQ2 = DI \times \sin(-\pi) + DQ \times \cos(-\pi)$

so as to shift the phase of a signal point indicated by the I signal component DI and the Q signal component DQ received from the latch 13 to the absolute phase, and transmits the I signal component $ADI1 = (-1) \times DI$ and the Q signal component $ADQ1 = (-1) \times DQ$ to the selective complex calculator circuit 21.

The selective complex calculator circuit 21 displaces the phase of a signal point indicated by the I signal component ADI1 and the Q signal component ADQ1 generated by absolute-phasing, in the absolute-phasing section 14, the I signal component DI and the Q signal component DQ by the phase Θ corresponding to the phase error signal (eight-phase phase error signal 8PPED, four-phase phase error signal QPPED, or two-phase phase error signal BPPED) generated by the filtering of the first to third filters 18

to 20, where the I signal component ADI1 and the Q signal component ADQ1 are represented by:

$ADI2 = ADI1 \times \cos\Theta - ADQ1 \times \sin\Theta$

$ADQ2 = ADI1 \times \sin\Theta + ADQ1 \times \cos\Theta$.

In accordance with the claimed invention, the phase of the signal point is corrected out of the carrier regenerating loop, and the regeneration of the carrier performed by receiving the burst regardless of the magnitude of the CNR enables elimination of the fluctuation of the error rate (BER) due to the phase noise of the ODU.

On the other hand, Shiraishi '921 appears to disclose a received-signal absolute-phasing apparatus used in a receiver, which adjusts the signal point arrangements of the received I and Q base-band signals of two series obtained by receiving and demodulating a signal to be PSK-modulated that carries at least an 8PSK-modulated digital signal among 8PSK-modulated digital signal, QPSK-modulated digital signal, and BPSK-modulated digital signal time-multiplexed with a BPSK-modulated frame synchronizing signal by a hierarchical transmission system such that the signal point arrangements of the received I and Q base-band signals coincides with that on the transmission side.

In the receiver of Shiraishi '921, the demodulating circuit 1 obtains I and Q base-band signals by quadrature-detecting an intermediate frequency signal IF. The demodulating circuit 1 comprises a carrier-wave regenerating circuit 10 for regenerating two reference carrier waves $f_{c1} = \cos(\omega t)$ of which the frequencies and phases synchronize with a received carrier wave and which is orthogonal to one another because their phases are shifted by 90° from one another, and multipliers for multiplying the intermediate frequency signal IF by f_{c1}, and f_{c2}.

The carrier-wave regenerating circuit 10 comprises a plurality of phase error tables 13, 14-1 and 14-2, and 15-1 to 15-4 respectively configured by a ROM and formed by tabulating the relations among the sets of the I and Q base-band signals I(8) and Q(8), and the carrier-wave phase error data having 8 quantized bits $\Delta\phi(8)$ for each

modulation system of 8PSK, QPSK and BPSK. The I and Q base-band signals I(8) and Q(8) are fed to the phase error tables 13, 14-1 and 14-2 and 15-1 to 15-4 in parallel. A phase error table selectively enabled by a selector 16 outputs the phase error data $\Delta\phi(8)$ corresponding to the I and Q base-band signals I(8) and Q(8) received from the demodulating circuit 1. The selector 16 enables, for example, only the phase error table 13 while the demodulating circuit 1 demodulates digital waves to be modulated in accordance with the BPSK modulation system in accordance with a clock CLK_{SYB} having a symbol rate synchronous with outputs of the I and Q base-band signals I(8) and Q(8) received from the demodulating circuit 1, and reads the phase error data $\Delta\phi(8)$ corresponding to the set data of the I(8) and Q(8) whenever the demodulating circuit 1 outputs the I and Q base-band signals I(8) and Q(8) for one symbol. When the phase error data $\Delta\phi(8)$ is equal to 0, the outputs of the LPF 18 are not changed or phases of the reference carrier wave f_{c1} and f_{c2} are not changed. When the phase error data $\Delta\phi(8)$ is positive, the outputs of the LPF 18 increase and phases of the reference carrier waves f_{c1} and f_{c2} are delayed. When the phase error data $\Delta\phi(8)$ is negative, the outputs of the LPF 18 decrease and phases of the reference carrier waves f_{c1} and f_{c2} are advanced.

Once the phase synchronization is established in accordance with the above procedure, the remapper 7 rotates the phases of the input I and Q base-band signals I(8) and Q(8) by an angle $\eta = -\Theta$ in accordance with the following formulas:

$$I' = I \times \cos(\eta) - Q \times \sin(\eta)$$

$$Q' = I \times \sin(\eta) + Q \times \cos(\eta)$$

and outputs the absolute-phased I and Q base-band signals I'(8) and Q'(8).

The Official Action asserts the following:

> The apparatus, shown in Fig. 12, regenerates a carrier by a carrier regeneration loop (10) and establishes phase synchronization to decode a PSK modulation signal regenerated from a modulated signal to a digital signal, where the phase of a signal point indicated by the PSK modulation signal outputted from said carrier regeneration loop is shifted (13, 14-1,

> 15-1, and 15-4) by a phase determined on the basis of the type of PSK modulation technique (ar(3)) applied to a received signal and a phase error contained in the PSK modulation signal, then the digital signal is decoded, and the carrier is regenerated on the basis of a phase error detected by performing burst receiving only in a predetermined signal interval (see Fig. 11A).

The Applicant respectfully disagrees and traverses the above-referenced assertions in the Official Action. The phase shift performed by using the phase error tables 13, 14-1 and 14-2, and 15-1 to 15-4 of Shiraishi '921 corresponds to the phase shift performed for establishing the phase synchronization in the carrier regeneration loop of the present invention, and the phase shift performed in the remapper 7 of Shiraishi '921 corresponds to the phase shift performed in the absolute-phasing section 14 of the present invention. Thus, Shiraishi '921 merely discloses the phase synchronization and the absolute-phasing of the present invention. Shiraishi '921 does not disclose the phase shift performed in the selective complex calculator circuit 21 of the present invention. Therefore, Shiraishi '921 does not disclose the feature of the present invention of shifting a phase of a signal point indicated, for example, by the I signal ADI1 and Q signal ADQ1, which are absolute-phased after the phase error or the frequency error have been compensated by the carrier regenerating loop, by the phase corresponding to the modulation technique applied to the received signal and the phase error amount. As a consequence, the received-signal absolute-phasing apparatus of Shiraishi '921 can neither enable a reduction in the effect on the error rate due to the phase noise of the outdoor unit (ODU), nor enable the stable receiving operation by performing the burst receiving at all times regardless of the magnitude of the carrier-to-noise ratio (CNR) and by regenerating the carrier.

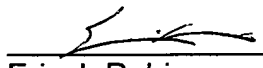
Therefore, Shiraishi '921 does not teach absolute-phasing a PSK modulation signal in which the phase of a signal point is adjusted by a carrier regenerated by a carrier regenerating loop, where a phase of a signal point indicated by the PSK modulation signal absolute-phased by the absolute-phasing means (or in the step of absolute-phasing a PSK modulation signal) is shifted by a phase determined on the

basis of the type of PSK modulation technique applied to a received signal and a phase error contained in the PSK modulation signal, then the digital signal is decoded, and the carrier is regenerated on the basis of a phase error detected by performing burst receiving only in a predetermined signal interval, either explicitly or inherently. Also, Shiraishi '921 does not teach phase shift means for shifting the phase of a signal point indicated by a PSK modulation signal absolute-phased by said absolute-phasing means by a phase determined on the basis of the type of PSK modulation technique applied to a received signal and a phase error contained in the PSK modulation signal, either explicitly or inherently.

Since Shiraishi '921 does not teach all the elements of the independent claims, either explicitly or inherently, an anticipation rejection cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 102 are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789